IN THE CLAIMS

Please amend the claims to be in the form as follows:

Claim 1 (previously presented): A transmission system comprising at least a station of a first type and a station of a second type which include a transmitting part having a transmit timing controller for transmitting data at a transmit timing and a receiving part having synchronizing circuits for synchronization with data transmitted from different station types to provide a receive timing, characterized in that the transmit timing is fixed in response to the receive timing characterized in that the receiving part of the station of the second type has a synchronization circuit that provide chip fractions shifted in time.

Claim 2 (previously presented): A transmission system as claimed in Claim 1, formed by a station of the first type where the receiving part comprising a synchronizing circuit for determining the receiving timing of a plurality of stations of the second type, characterized in that the synchronizing circuit of the station of the first type is known to all the stations of the second type.

ok to enter RMM 2/2/05

Claim 3 (previously presented): A transmission system as claimed in Claim 1 characterized in that the stations of the second type comprise means for evaluating a frequency shift, of the receiving frequency relative to the transmitting frequency of the station of the first type and means for modifying the transmitting frequency of the station of the second type as a function of this frequency deviation.

Claim 4 (previously presented): A transmission system comprising at least a station of a first type and a station of a second type which include a transmitting part having a transmit timing controller for transmitting data at a transmit timing and a receiving part having synchronizing circuits for synchronization with data transmitted from different station types to provide a receive timing, characterized in that the receiving part of the station of the second type has a synchronization circuit that provide chip fractions shifted in time and the station of the first type comprises a receiving circuit to be shared by all the stations of the second type to which it is connected.

Claim 5 (previously presented): A synchronization method suitable for a system comprising at least a station of a first type and a station of a second type which include a transmitting part having a transmit timing controller for transmitting data at a transmit timing and a receiving part having synchronizing circuits for synchronization with data transmitted from different station types to provide a receive timing, characterized in that it comprises the following steps:

- providing the receiving part of the station of the second type with a synchronization circuit that generates chip fractions shifted in time,
- measuring the receive clock derivation made at the stations of the second type,
- comparing the transmit clock at the station of the second type by adopting the opposite deviation value,
-
- single synchronization of the receive clock at the station of the first type.

Claim ~~5~~ 6 (currently amended): A transmission system as claimed in Claim 1, wherein the synchronization circuit provides chip fractions shifted in time produces a first output corresponding to a satisfactory state of synchronism.

Claim ~~6~~ 7 (currently amended): A transmission system as claimed in Claim ~~5~~ 6, wherein the synchronization circuit provides chip fractions shifted in time produces an already produced chip fraction output that contains chip fraction previously produced at the first output.

Claim ~~7~~ 8 (currently amended): A transmission system as claimed in Claim ~~6~~ 7, wherein the synchronization circuit provides chip fractions shifted in time produces a recently produced chip fraction output that contains chip fraction that have just been produced.

Claim ~~8~~ 9 (currently amended): A transmission system as claimed in Claim ~~7~~ 8, wherein the receiving part of the station of the second type further comprises an analysis circuit receives chip fractions shifted in time by the synchronization circuit and determines a frequency drift, therefrom.

Claim ~~9~~ 10 (currently amended): A transmission system as claimed in Claim ~~8~~ 9, wherein the receiving part of the station of the second type further comprises means for modifying clock frequencies in response to the frequency drift.

Claim ~~10~~ 11 (currently amended): A transmission system as claimed in Claim 4, wherein the synchronization circuit provides chip fractions shifted in time produces a first output corresponding to a satisfactory state of synchronism.

Claim ~~11~~ 12 (currently amended): A transmission system as claimed in Claim ~~10~~ 11, wherein the synchronization circuit provides chip fractions shifted in time produces an already produced chip fraction output that contains chip fraction previously produced at the first output.

Claim ~~12~~ 13 (currently amended): A transmission system as claimed in Claim ~~11~~ 12, wherein the synchronization circuit provides chip fractions shifted in time produces a recently produced chip fraction output that contains chip fraction that have just been produced.

Claim ~~13~~ 14 (currently amended): A transmission system as claimed in Claim ~~12~~ 13, wherein the receiving part of the station of the second type further comprises an analysis circuit receives chip fractions shifted in time by the synchronization circuit and determines a frequency drift, therefrom.

Claim ~~14~~ 15 (currently amended): A transmission system as claimed in Claim ~~13~~ 14, wherein the receiving part of the station of the second type further comprises means for modifying clock frequencies in response to the frequency drift.

Claim ~~15~~ 16 (currently amended): A method as claimed in Claim 5, wherein the synchronization circuit provides chip fractions shifted in time produces a first output corresponding to a satisfactory state of synchronism.

Claim ~~16~~ 17 (currently amended): A method as claimed in Claim ~~15~~ 16, wherein the synchronization circuit provides chip fractions shifted in time produces an already produced chip

fraction output that contains chip fraction previously produced at the first output.

Claim ~~17~~ 18 (currently amended): A method as claimed in Claim ~~16~~ 17, wherein the synchronization circuit provides chip fractions shifted in time produces a recently produced chip fraction output that contains chip fraction that have just been produced.

Claim ~~18~~ 19 (currently amended): A method as claimed in Claim ~~17~~ 18, wherein the receiving part of the station of the second type further comprises an analysis circuit receives chip fractions shifted in time by the synchronization circuit and determines a frequency drift, therefrom.

Claim ~~19~~ 20 (currently amended): A method as claimed in Claim ~~18~~ 19, wherein the receiving part of the station of the second type further comprises means for modifying clock frequencies in response to the frequency drift.